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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Yi-Fan Chen, Examiner: Huynh, Andy
5 Chi-King Pu,
Shou-Kong Fan

Filing Date: 04/18/01 Art Unit: 2818
Serial No.: 09/836,258 Docket No.: NAUP0280USA

10 Title: BYPASS CIRCUITS FOR REDUCING PLASMA DAMAGE

To: The Commissioner of Patents and Trademarks
Washington, D.C. 20231

15 Subject: Response to the Office Action dated 05/03/2002

Dear Sir:

AMENDMENT

20

In response to the Office Action identified above,
please amend the above-identified application as
follows:

25 In the claims:

1. (Once amended) A bypass circuit for reducing plasma
damage to a gate oxide of a metal-oxide semiconductor
(MOS) wafer, the bypass circuit positioned on a
semiconductor wafer, the semiconductor wafer
30 comprising a substrate, the MOS transistor, a
dielectric layer, and the bypass circuit, respectively,
with the bypass circuit comprising:

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